Serial No.: 10/689,923
Group Art Unit: 2823

AMENDMENTS TO CLAIMS

- Please cancel claims 1, 2, 5, 6, and 11–20 without prejudice.

Claims 1-6. (Cancelled).

7. (Previously Presented) A method for manufacturing an integrated circuit structure, comprising:

providing a semiconductor substrate;

forming an oxide-nitride-oxide dielectric layer on the semiconductor substrate;

forming a layer of polysilicon on the oxide-nitride-oxide dielectric layer;

forming a nitride hardmask layer on the layer of polysilicon;

patterning and forming a composite mask on the nitride hardmask;

etching the nitride hardmask, layer of polysilicon, oxide-nitride-oxide dielectric layer, and semiconductor substrate to form shallow trench isolation trenches;

filling the shallow trench isolation trenches with an oxide gap fill;

polishing the oxide gap fill;

removing the nitride hardmask;

covering an array area over the semiconductor substrate with a photoresist mask;

removing the polysilicon and the oxide-nitride-oxide dielectric in a periphery area;

performing well and threshold implantation over the periphery area into the semiconductor substrate;

covering the periphery area over the semiconductor substrate with a photoresist mask; and

performing well and threshold implantation over the array area above the semiconductor substrate into the semiconductor substrate beneath the oxide-nitride-oxide dielectric layer.

8. (Original) The method of claim 7 further comprising forming a channel implantation over the array area and the periphery area into the semiconductor substrate therebeneath.

9. (Original) The method of claim 8 further comprising:

forming a gate dielectric layer over at least portions of the periphery area;

forming at least one control gate layer over at least portions of the gate dielectric layer; and

forming an interlayer dielectric layer over at least portions of the array area and the periphery area.

10. (Original) The method of claim 9 further comprising forming at least one electrical contact through the interlayer dielectric layer to at least one portion of the control gate layer therebeneath, and at least one electrical contact through the interlayer dielectric layer to at least one portion of the polysilicon therebeneath.

Claims 11-20. (Cancelled).